At page 3 of the Office Action, the Examiner indicates that claims 11-15 and 18-19 are allowed. Applicant sincerely and earnestly thanks the Examiner for the indication of allowable subject matter.

At page 2 of the Office Action, the Examiner objects to the drawings. In response, Applicant is submitting a Request For Approval of Drawing Correction with proposed changes to the Figures. The changes are also reflected in the formal drawings that are being concurrently filed herewith. The set of formal drawings should address the other objections to the drawings. Withdrawal of the objection is requested.

At page 2 of the Office Action, the Examiner objects to phrase "invisible lines" in the specification. In response, Applicant has changed the phrase "invisible lines" to --dotted lines-- in the specification. Withdrawal of the objection is requested.

At page 3 of the Office Action, claims 1-10 and 16-17 are rejected as being indefinite.

The Examiner objects to the phrase "covering a portion the first surface", because it is allegedly unclear. In response, claim 1 is amended to recite --covering a portion of the first surface--.

The Examiner also objects to the phrase "wherein gate is a trenched gate" in claim 10. In response, claim 10 is amended to recite --wherein the gate is a trenched gate--.

Lastly, the Examiner states "[c]laim 16 recites a bus member electrically coupling the source region to the ground plane. What source region?" In response, in claim 16, the phrase "source region" is replaced with --emitter region--.

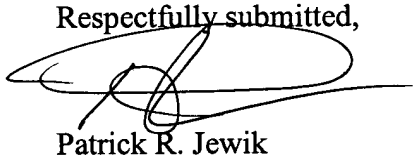
As each of the objections to claims 1, 10, and 16 have been addressed by Applicant, it is believed that claims 1-19 are in condition for allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph at page 1, line 10 has been amended as follows.

[03] A simplified illustration of a portion of an LDMOS RF power transistor package is shown in FIG. 1. FIG. 1 shows a semiconductor die **11** with an N+ source region **12** and an N+ drain region **17** at the top surface. The source region **12** electrically connects to a source electrode **S** at the bottom surface of the semiconductor die **11.** A P+ region **14** provides a conductive path to the N+ source region **12.** A metal portion **18** shorts out a p+ body region **19** and the N+ source region **12** to provide an electrical path between the source region **12** to the source electrode **S.** A drain electrode **D** and a gate **G** are also at the top surface of the semiconductor die **11.** For clarity of illustration, the gate oxide corresponding to the gate **G** is not shown in FIG. 1. The source electrode **S** at bottom surface of semiconductor die **11** is attached to a metallic substrate **13.** The metallic substrate **13** serves as both a heat sink and a ground reference for the source electrode **S.** Wires (not shown) are coupled to the gate electrode **G** and the drain electrode **D** to provide the semiconductor die **11** with input and output connections. In operation, source current flows from the metallic substrate **13,** laterally through the drift region **16** to the drain region **17,** and out of the semiconductor die **11** to a wire (not shown) coupled to the drain electrode **D.**

The paragraph at page 2, line 12, has been amended as follows.

[08] One embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface; a source region at

the first surface of the semiconductor die; a gate at the first surface of the semiconductor die; a drain region at the second surface of the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.

The paragraph beginning at page 3, line 1 has been amended as follows:

[10] Another embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface; an emitter region at the first surface of the semiconductor die; a base region at the first surface of the semiconductor die; a collector region at the second surface of the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the [source] emitter region of the semiconductor die to the ground plane.

The paragraph beginning at page 3, line 9 has been amended as follows:

[11] Another embodiment of the invention is directed to a semiconductor die package comprising: a semiconductor die comprising a transistor, wherein the semiconductor die has a first surface and a second surface; a source region in the semiconductor die; a gate in the semiconductor die; a drain region in the semiconductor die; a ground plane proximate the second surface and distal to the first surface; and a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.

The paragraph beginning at page 3, line 28 has been amended as follows:

[16] FIG. 4 shows a top view of a portion of a semiconductor package according to an embodiment of the invention. [The bus member is shown by invisible lines.]

The paragraph beginning at page 6, line 10 has been amended as follows:

[32] The bus members according to embodiments of the invention can have flat portions that form angles. For instance, the bus member **26** shown in FIG. 2 has a horizontal portion coupled to the source region **126** of the semiconductor die **30** and at least one leg that extends downward toward the ground plane **20**. Preferably, the bus member **26** has two (or more) legs that extend to the ground plane **20** at opposite ends of the semiconductor die **30**. The bus member **26** electrically couples the ground plane **20** to the source region **126**. One leg is shown by the [invisible] dotted lines in FIG. 2. In some embodiments, the horizontal portion of the bus member **26** can be a continuous body of metal and can cover a major portion of the first surface **31(a)** of the semiconductor die **30** (e.g., greater than 50% of the area of the first surface **31(a)**). Solder in the form of hemispherically shaped logs, balls, columns, etc. can be used to electrically couple the horizontal portion of the bus member **26** to various source region connections at the first surface **31(a)** of the semiconductor die **30**. Solder can also be used to couple the ends of the one or more legs of the bus member **26** to the ground plane **20**.

The paragraph beginning at page 7, line 12 has been amended as follows:

[36] FIG. 4 shows a top plan view a portion a semiconductor die package with the inner leg surface of the bus member **26** shown by [invisible] dotted